amplifier output power **226** will first go down, and than will go back to its original setpoint value of 16 dBm (40 mW). In this case the transition time is close to 0.5 mseconds.

The exemplary amplifier **100** of the present invention has a controller **120** with a capability of output power and gain transient suppression and temperature control of the laser pump diode. Control requirements, such as set point and control mode are remotely sent to the amplifier **100** via standard interface (serial, parallel or Ethernet). Monitoring signal and alarms from the amplifier are received by using the same interface. Two embedded processors allow high level of flexibility in the choice of control and processing algorithms. The technique of signal compression and dynamic range switching makes this device suitable for use in systems with very wide dynamic range of signals. This particular amplifier **100** utilizes two independently controlled pump lasers. The second pump is used to boost the signal power. The controller **120** may also utilize more sophisticated control algorithms, which can cope with some long-term effects, such as parameter changes caused by the optical component aging.

Accordingly, it will be apparent to those skilled in the art that various modifications and adaptations can be made to the present invention without departing from the spirit and scope of the invention. For example, the controller **120** can be utilized with non-erbium- doped fiber amplifiers, for example, Tm-doped amplifiers. It may also be utilized in amplification systems that include Raman amplifiers, or planar waveguide amplifiers. It is intended that the present invention covers the modifications and adaptations of this invention as defined by the appended claims and their equivalents.

What is claimed is

1. An amplifier characterized by gain and output power comprising:
   (i) at least one gain medium;
   (ii) at least one pump supplying optical power into said gain medium;
   (iii) a controller controlling said gain and said output power of said amplifier, said controller including a signal compression circuit to cover a wide dynamic range for optical input and output signals, so that resolution for low optical signals is better than resolution for high optical signals.

2. The amplifier according to claim 1, wherein said gain medium includes at-least one coil of rare earth doped fiber.

3. The amplifier of claim 1, wherein said controller utilizes a logarithmic circuit.

4. The amplifier of claim 1, wherein said controller electronic gain switch circuit.

5. The amplifier of claim 2, wherein said controller utilizes a logarithmic circuit.

6. The amplifier of claim 2, wherein said controller electronic gain switch circuit.

7. The amplifier of claim 1, wherein said controller utilizes at least two feedback loops, one of said loops being a fast loop and another one of said feedback loops being a slow loop, wherein said slow loop operates in the range of 1 Hz to 10 kHz, and said fast loop operates in the range of 500KHz to 10Mhz.

8. The amplifier of claim 7,wherein said fast loop is pump power control loop, and said slow loop is pump temperature control loop.

9. The amplifier of claim 8, said slow loop is also temperature control loop of rare-earth doped fiber.

10. The amplifier of claim 1, wherein said controller utilizes only a slow control loop, said slow control operating in the range of 1-1000 Hz, and does not control power transients.

11. An amplifier characterized by gain and output power comprising:
(i) gain medium including rare earth-doped fiber;
(ii) a pump supplying optical power into said gain medium;
(iii) a controller controlling said gain and said output power of said amplifier, said controller including an electronic gain switch to cover a wide dynamic range for optical input and output signals, so that resolution for low optical signals is better than resolution for high optical signals.

12. The amplifier of claim 11, wherein said controller includes (i) an A/D converter, and (ii) an electronic gain switch, said electronic gain switch detects the level of electrical signal corresponding to optical signal level and, when said electrical signal is lower then a predetermined amount, and multiplies that signal by a predetermined constant, providing this multiplied signal to A/D converter.

13. The amplifier of claim 11, wherein said controller includes (i) an A/D converter, and (ii) an electronic gain switch, said gain switch said electronic gain switch detects the level of electrical signal corresponding to optical signal level and, when said electrical signal is higher then a predetermined amount for a predetermined period of time, and lowers the electronic gain, provided by the electronic gain switch, so that the input to the A/D converter stays within its range, thereby preventing an overflow condition.

14. An amplifier according to claims 2, 4 and 13, wherein said electronic gain switch includes a circuit that utilizes hysteresis to prevent unwanted electronic gain switch oscillation.

15. The amplifier of claim 1, furthers comprising A/D converter that can convert multiple analog signals simultaneously into multiple digital signals.

16. The amplifier of claim 15, wherein one of said analog signals corresponds to optical input power and the other one of said analog signals corresponds to the optical output power.

5

17. The amplifier of claim 1, wherein said controller incorporates an automatic gain control, coil temperature and pump temperature control system and a communication/alarm processing system.

10

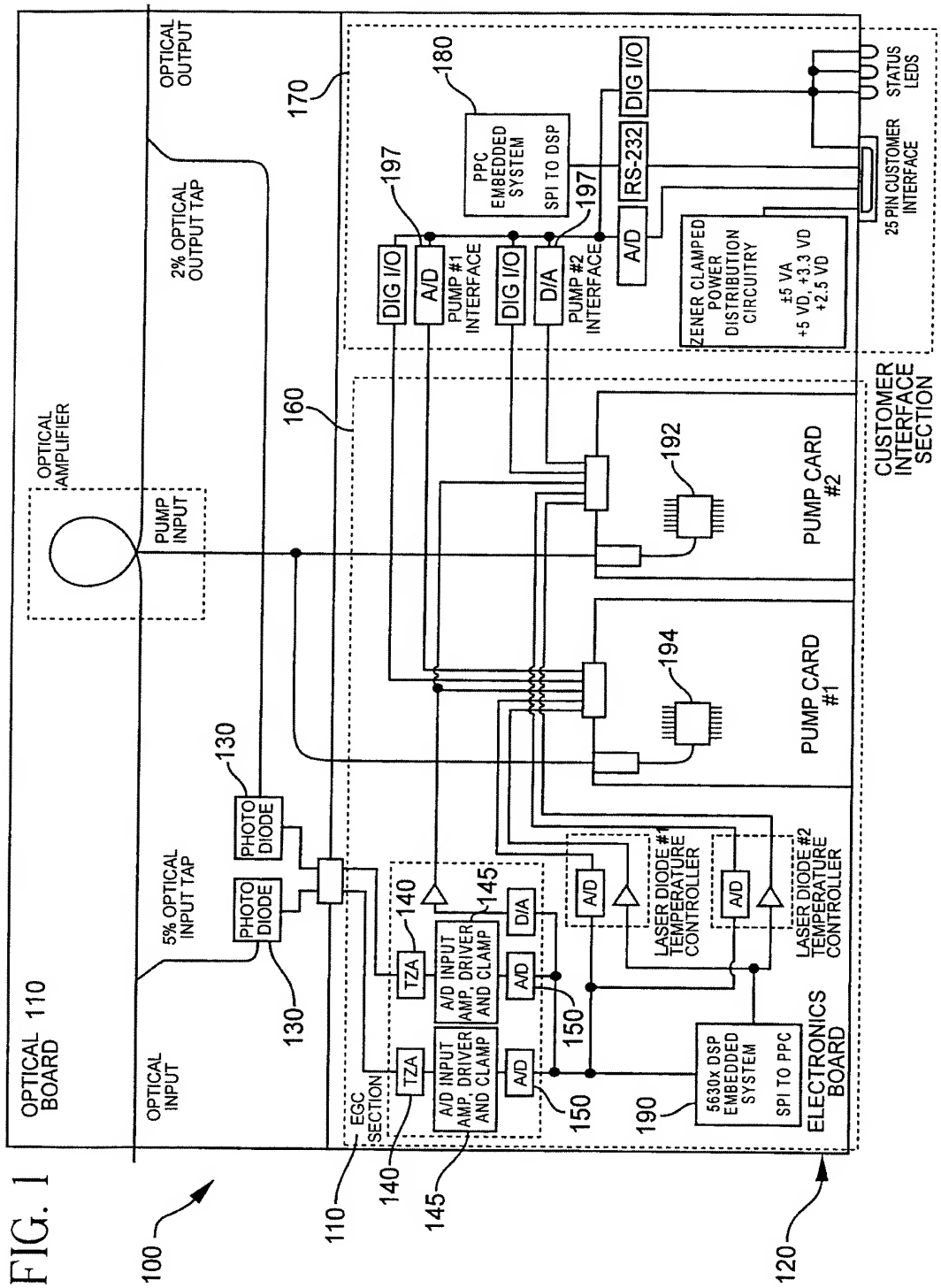

OPTICAL BOARD 110
OPTICAL INPUT
OPTICAL AMPLIFIER
PUMP INPUT
OPTICAL OUTPUT
2% OPTICAL OUTPUT TAP
5% OPTICAL INPUT TAP
PHOTO DIODE
PHOTO DIODE
130
130
EGC SECTION
TZA
TZA
A/D INPUT AMP, DRIVER AND CLAMP
A/D INPUT AMP, DRIVER AND CLAMP
140
145
D/A
A/D
A/D
A/D
150
150
LASER DIODE #1 TEMPERATURE CONTROLLER
LASER DIODE #2 TEMPERATURE CONTROLLER
5630x DSP EMBEDDED SYSTEM
SPI TO PPC
190
ELECTRONICS BOARD
120
100
110
140
145
160
PUMP CARD #1
194
PUMP CARD #2
192
CUSTOMER INTERFACE SECTION
170
180
PPC EMBEDDED SYSTEM
SPI TO DSP
197
197
DIG I/O
A/D
PUMP #1 INTERFACE
DIG I/O
D/A
PUMP #2 INTERFACE
A/D
DIG I/O
RS-232
ZENER CLAMPED POWER DISTRIBUTION CIRCUITRY
±5 VA
+5 VD, +3.3 VD
+2.5 VD
25 PIN CUSTOMER INTERFACE
STATUS LEDS

FIG. 1

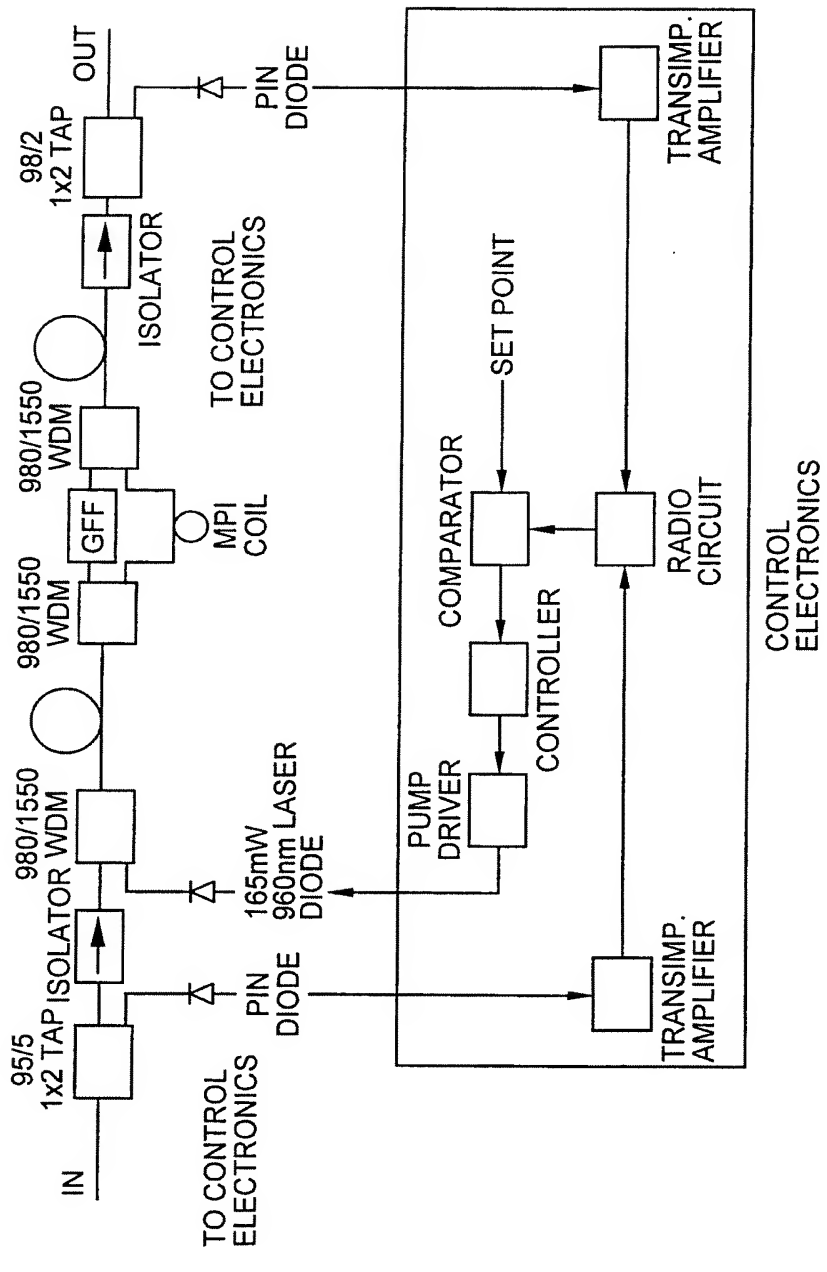

IN
95/5
1x2 TAP
ISOLATOR
980/1550
WDM
980/1550
WDM
GFF
980/1550
WDM
ISOLATOR
98/2
1x2 TAP
OUT
TO CONTROL
ELECTRONICS
PIN
DIODE
165mW
960nm LASER
DIODE
MPI
COIL
TO CONTROL
ELECTRONICS
PIN
DIODE
PUMP
DRIVER
CONTROLLER
COMPARATOR
SET POINT
TRANSIMP.
AMPLIFIER
RADIO
CIRCUIT
TRANSIMP.
AMPLIFIER
CONTROL
ELECTRONICS

FIG. 2

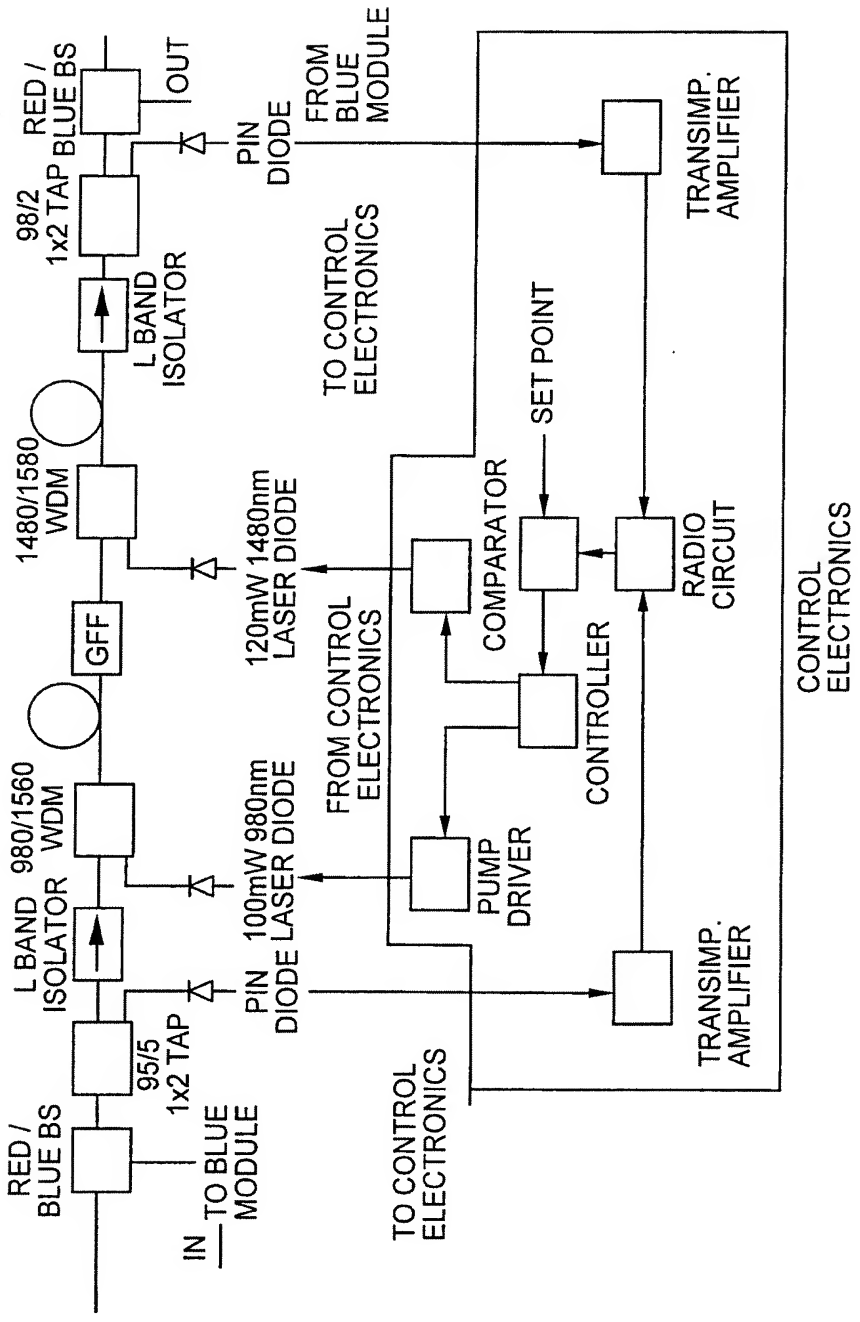

RED / BLUE BS
IN
TO BLUE MODULE
95/5 1x2 TAP
L BAND ISOLATOR
980/1560 WDM
GFF
1480/1580 WDM
L BAND ISOLATOR
98/2 1x2 TAP
RED / BLUE BS
OUT
PIN DIODE
100mW 980nm LASER DIODE
120mW 1480nm LASER DIODE
PIN DIODE
FROM BLUE MODULE
TO CONTROL ELECTRONICS
FROM CONTROL ELECTRONICS
PUMP DRIVER
COMPARATOR
SET POINT
CONTROLLER
RADIO CIRCUIT
TRANSIMP. AMPLIFIER
TRANSIMP. AMPLIFIER
TO CONTROL ELECTRONICS
CONTROL ELECTRONICS

FIG. 3

FIG. 4A

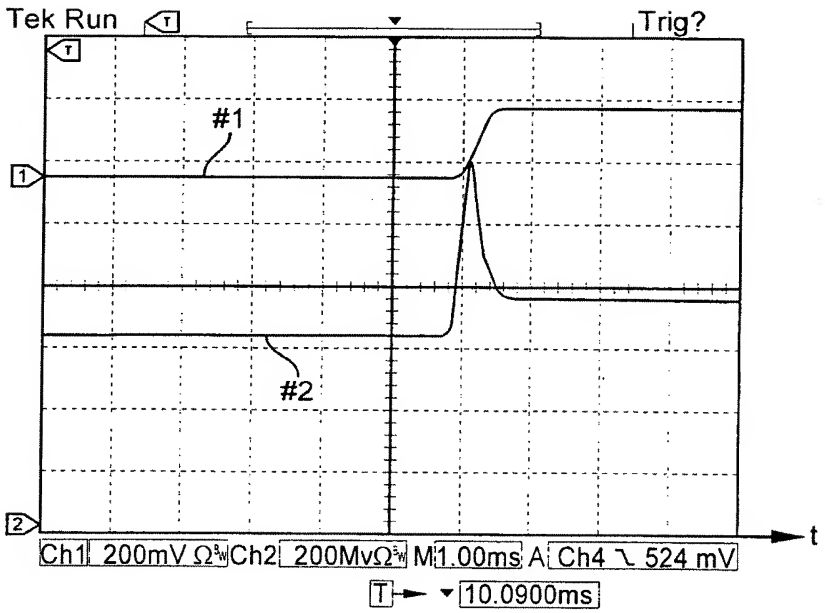

Tek Run
Trig?
#1
#2
t
Ch1 200mV Ω
Ch2 200MvΩ
M 1.00ms A Ch4 ⌥ 524 mV
10.0900ms

FIG. 4B

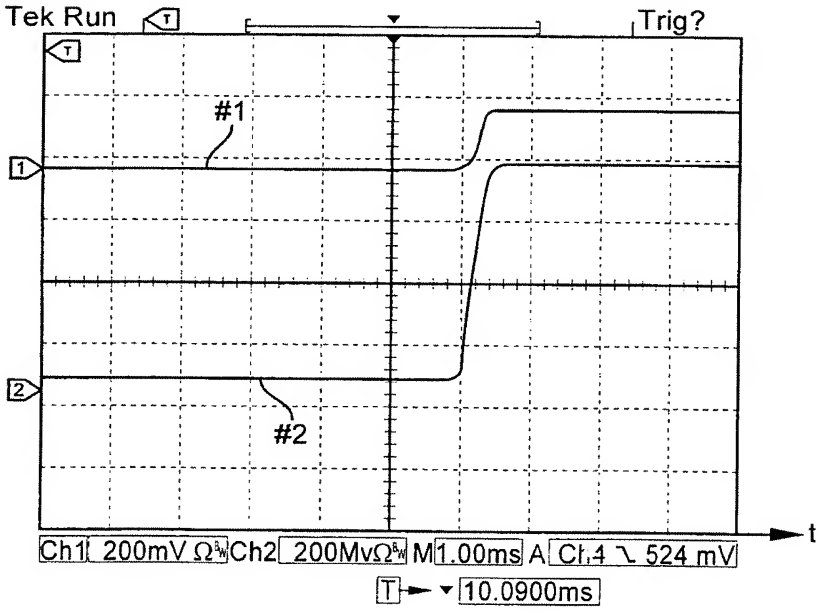

Tek Run
Trig?
#1
#2
t
Ch1 200mV Ω
Ch2 200MvΩ
M 1.00ms A Ch4 ⌥ 524 mV
10.0900ms

FIG. 4C

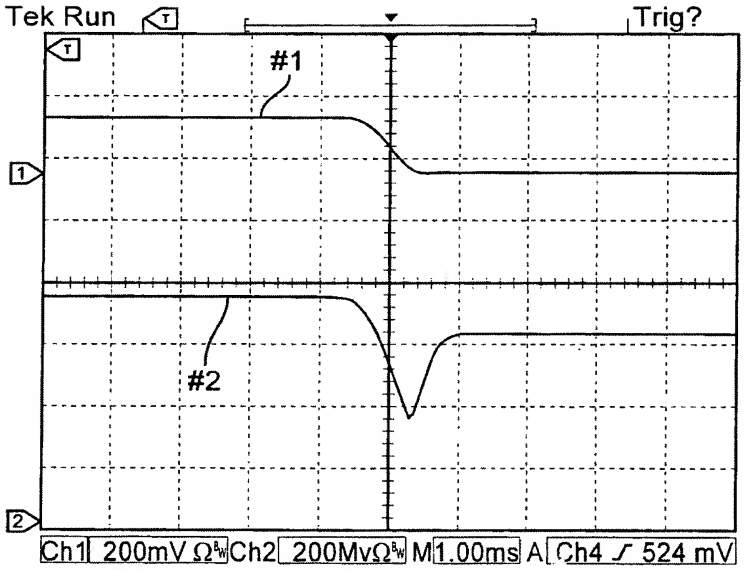

Tek Run
Trig?
#1
#2
Ch1 200mV Ω
Ch2 200MvΩ
M 1.00ms
A Ch4 524 mV

FIG. 4D

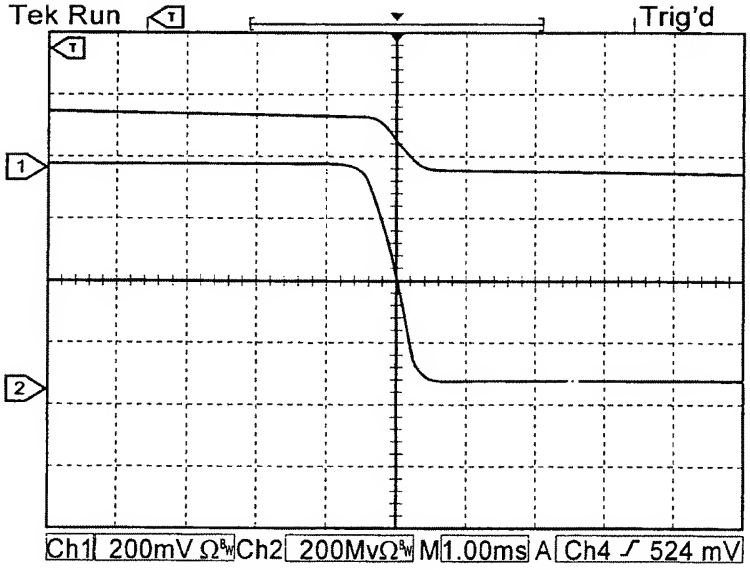

Tek Run
Trig'd
Ch1 200mV Ω
Ch2 200MvΩ
M 1.00ms
A Ch4 524 mV

FIG. 5A

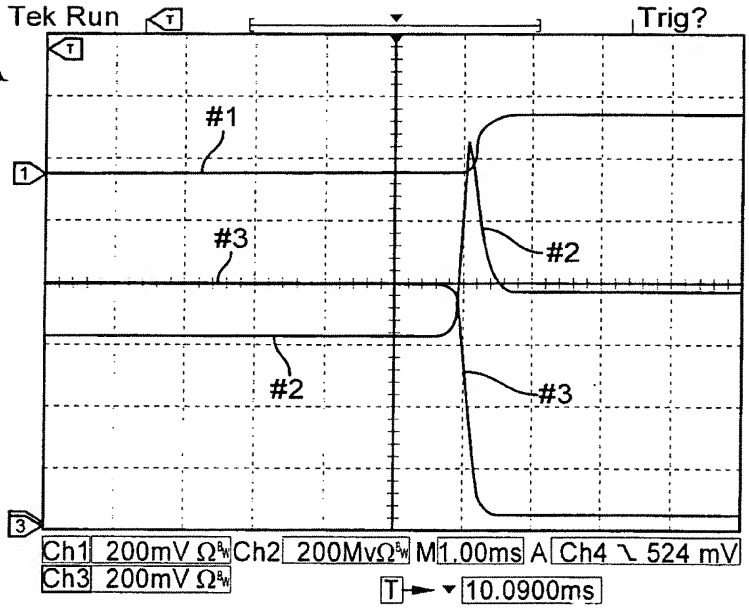

Tek Run
Trig?
#1
#2
#3
#2
#3
Ch1 200mV Ω
Ch2 200MvΩ
M 1.00ms A Ch4 ∖ 524 mV
Ch3 200mV Ω
10.0900ms

FIG. 5B

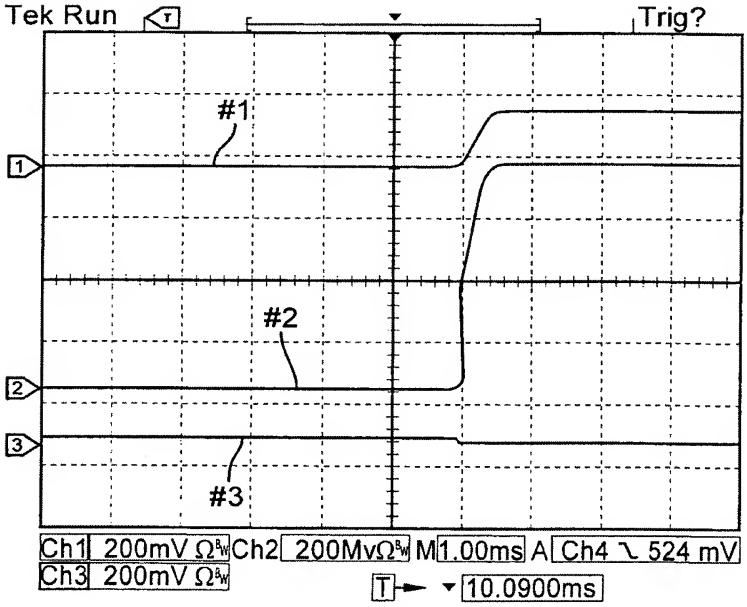

Tek Run
Trig?
#1
#2
#3
Ch1 200mV Ω
Ch2 200MvΩ
M 1.00ms A Ch4 ∖ 524 mV
Ch3 200mV Ω
10.0900ms

FIG. 5C

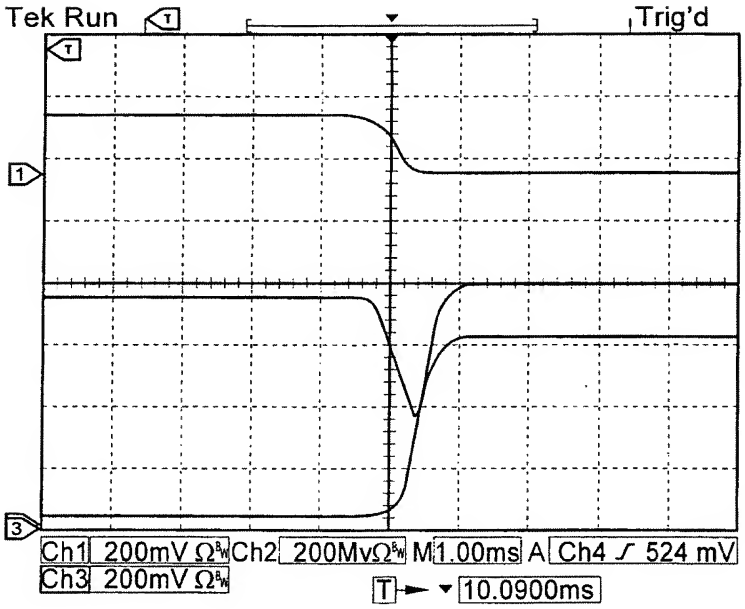
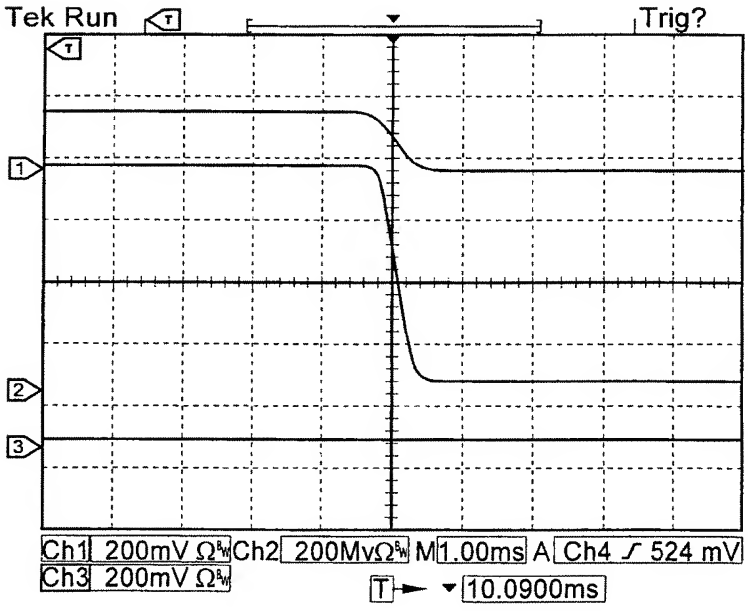

Tek Run
Trig'd
Ch1 200mV Ω
Ch2 200MvΩ
M 1.00ms A Ch4 524 mV
Ch3 200mV Ω
10.0900ms

FIG. 5D


Tek Run
Trig?
Ch1 200mV Ω
Ch2 200MvΩ
M 1.00ms A Ch4 524 mV
Ch3 200mV Ω
10.0900ms

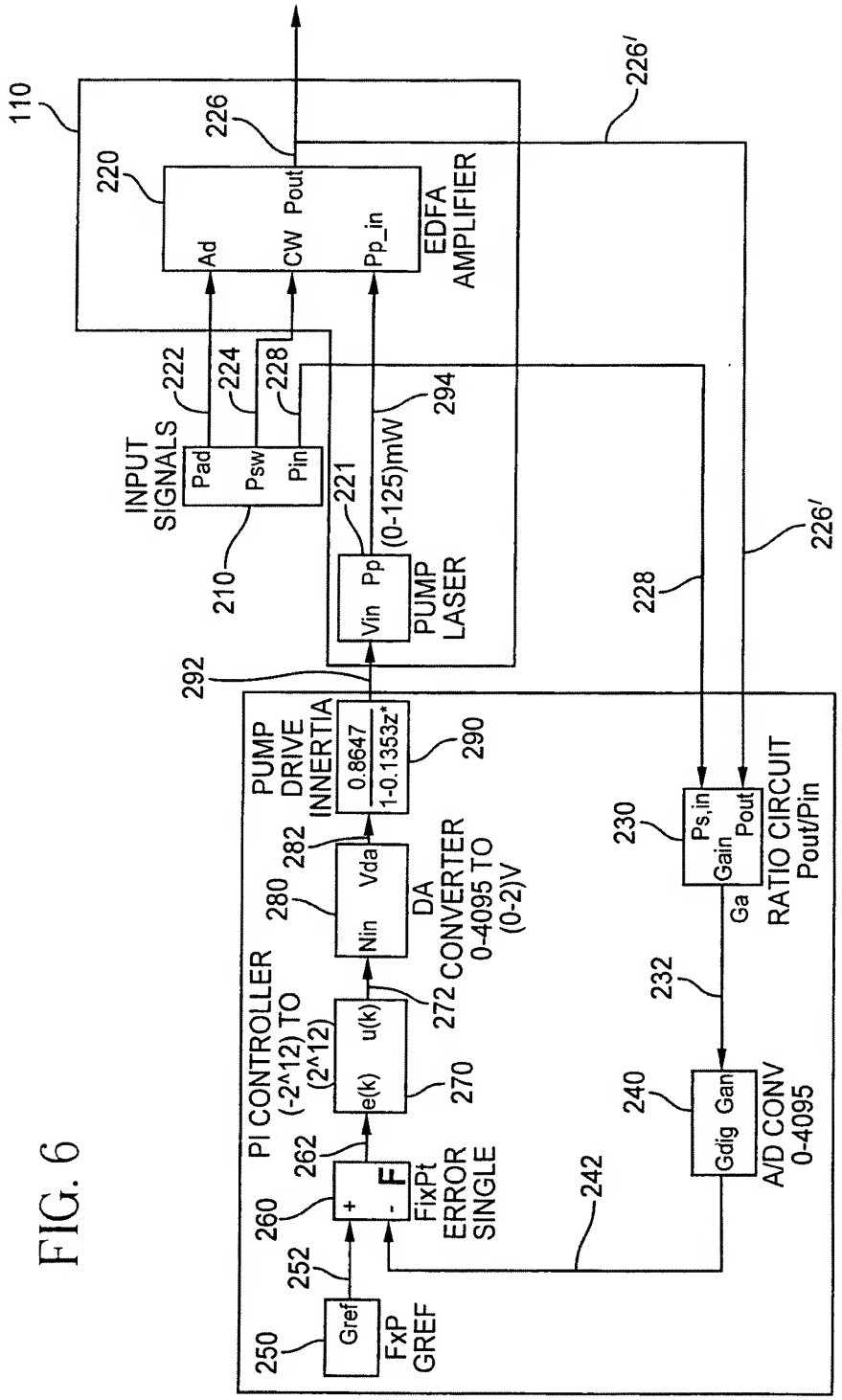

110
220
226
226'
Ad
CW Pout
Pp_in
EDFA AMPLIFIER
222
224
228
294
INPUT SIGNALS
Pad
Psw
Pin
221
(0-125)mW
210
Vin Pp
PUMP LASER
292
228
226'
PUMP DRIVE INNERTIA
0.8647
1-0.1353z⁻¹
290
230
Ps,in
Gain
Pout
RATIO CIRCUIT Pout/Pin
282
280
Vda
Nin
DA CONVERTER 0-4095 TO (0-2)V
Ga
232
PI CONTROLLER (-2^12) TO (2^12)
272
u(k)
e(k)
270
240
Gdig Gan
A/D CONV 0-4095
262
260
+
-
F
FixPt ERROR SINGLE
242
252
250
Gref
FxP GREF

FIG. 6

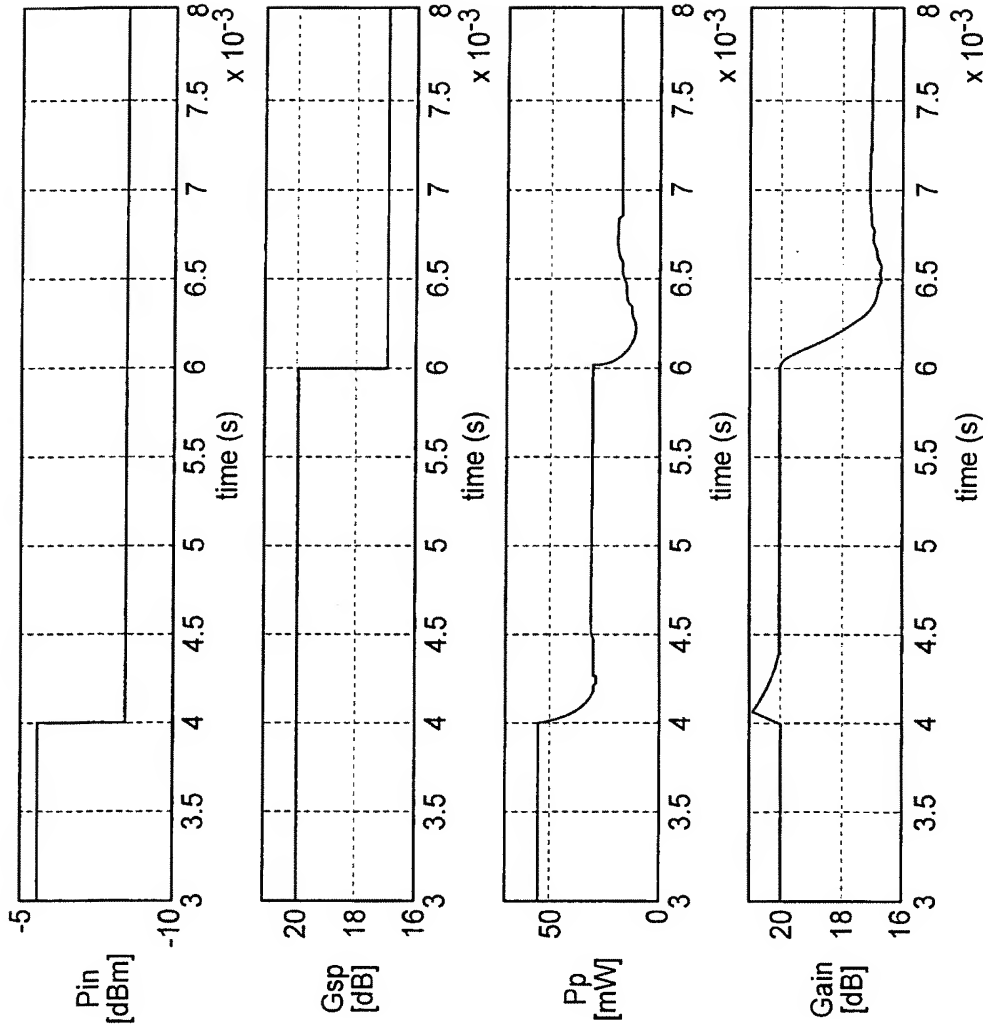


FIG. 7A

FIG. 7B

FIG. 7C

FIG. 7D

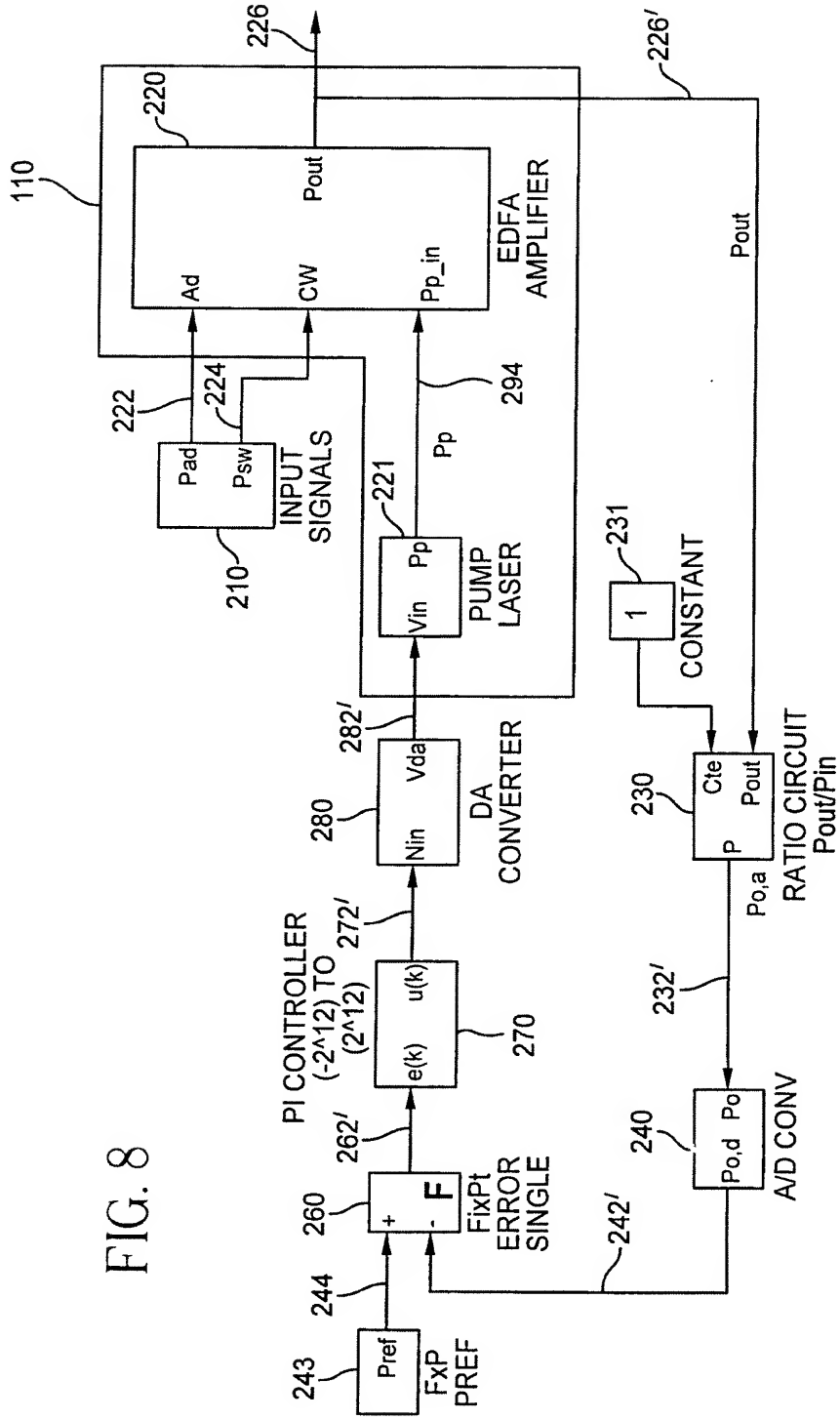

110
220
226
226'
Pout
Ad
CW
Pp_in
EDFA AMPLIFIER
222
224
294
Pad
Psw
INPUT SIGNALS
210
221
Pp
Vin
PUMP LASER
231
1
CONSTANT
282'
280
Vda
Nin
DA CONVERTER
230
Cte
Pout
P
RATIO CIRCUIT Pout/Pin
Po,a
272'
PI CONTROLLER (-2^12) TO (2^12)
u(k)
e(k)
270
232'
262'
260
+
-
F
FixPt ERROR SINGLE
240
Po,d
Po
A/D CONV
242'
244
243
Pref
FxP PREF

FIG. 8

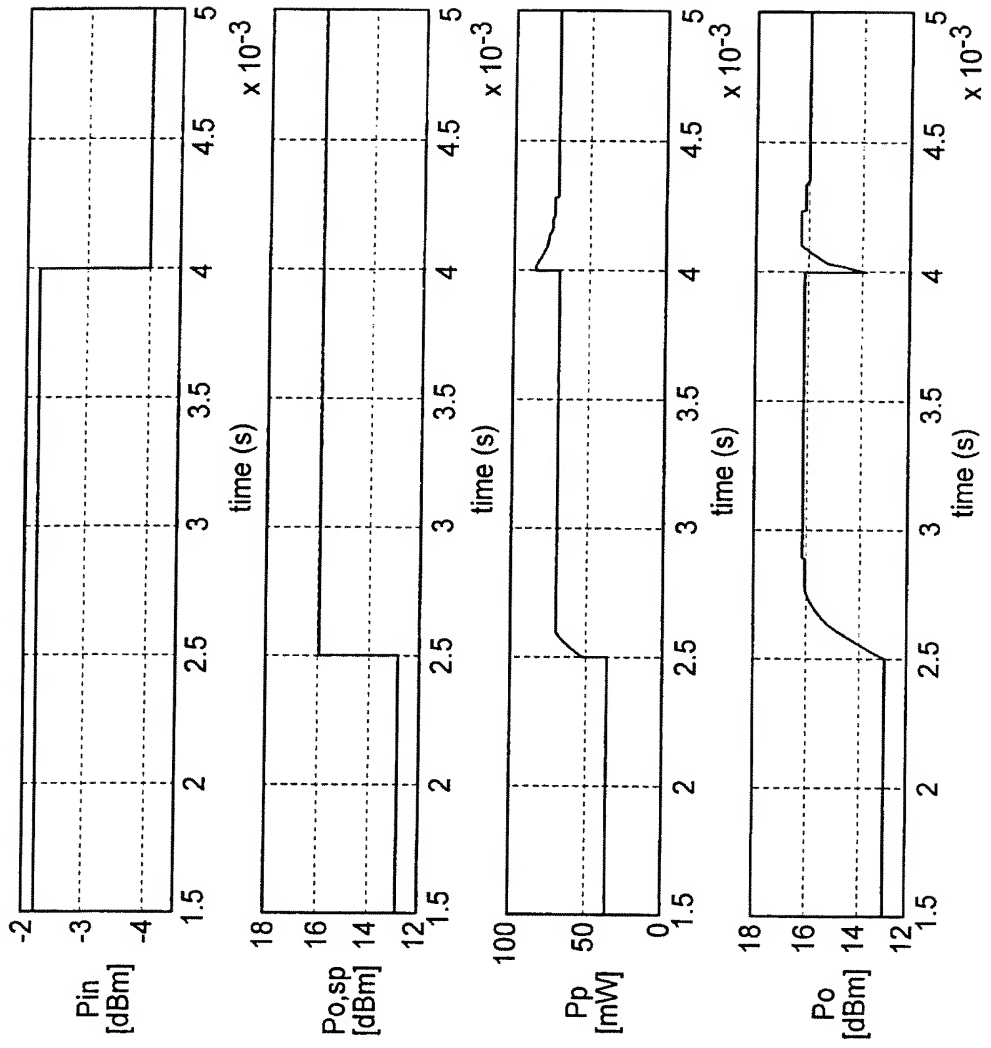


FIG. 9A

FIG. 9B

FIG. 9C

FIG. 9D

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US01/06026

A. CLASSIFICATION OF SUBJECT MATTER
IPC(7) : H01S 3/00
US CL : 359/341.3, 341.4, 341.41
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 359/341.3, 341.4, 341.41

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5,923,462 A (VAN DER PLAATS) 13 July 1999, Figure 1	1-17
Y	US 5,703,711 A (HAMADA) 30 December 1997, Figure 1	1-17
Y	US 5,363,385 A (HEIDEMANN) 08 November 1994, Figures 1 and 2.	8, 9 and 17

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
16 August 2001 (16.08.2001)	10 OCT 2001
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. 703 305-3230	Authorized officer MARK HELLNER Telephone No. 703 306-4155

Form PCT/ISA/210 (second sheet) (July 1998)